

# John Webster

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## Summary

Full stack developer with 30 years experience in computer industry looking for challenging and rewarding work in web design in the Folsom/Sacramento area

Full stack is a natural fit for me as it requires continuous research to be successful, learning multiple languages, flows, interfaces and design patterns. This is analogous to my work in chip design, where the underlying technology changes every 2 years, usually with changes in tools and requirements. I love to be able to apply knowledge from several domains in solving problems

I get the most job satisfaction from people using something I have helped build.

## Links

LinkedIn : [www.Linkedin.com/in/JohnWWebster](http://www.Linkedin.com/in/JohnWWebster)

Github: <https://github.com/johnlobster>

Portfolio: <https://johnlobster.github.io/portfolio/>

## March-August 2019 : UC Davis bootcamp – Full stack web development

### Key full stack technologies

MERN – MongoDB, Express, React, Node  
HTML, CSS, Javascript, mySQL, git

### Other libraries/technologies

Vscode, Trello, npm, mongoose, sequelize, handlebars, lodash, mocha, chai, chai-http, postman, bcrypt, react-router, cheerio, moment, sass, jsonwebtoken, winston, bootstrap, materialize, create-react-app, JQuery, github, travisCI, heroku, eslint, axios, firebase, bash, json, ajax, REST, API, bash, typescript

### Professional skills

- Managed small teams (to 5 people). Mentored junior engineers.
- Delivered technical training to team and taught Intel core values classes
- Worked in teams across sites and geographies
- Results focused ability to rapidly learn or develop new methodologies, tools and flows
- Data-driven approach to debugging

### Work history

#### Intel Corporation (Folsom, CA) September 1996 – July 2015. Senior component design engineer

2007 - 2015 Integrated graphics (VPG) – Technology team, part of physical design team

- VPG supplies integrated graphics for Intel CPUs using ASIC methodologies.
- Designed and analyzed power grid for all for integrated graphics products – re-used on many other ASIC products within Intel
- First tapeouts on 22nm (Haswell), 14nm (Broadwell), 10nm (CanonLake).

- Designed metal patterns/stack as part of Intel process definition team, generating reliability trade offs, density trade offs, library design trade offs (Intel award)
  - Designed power gate placement and connection scheme - analysis of area impact and Electromigration
  - Local expert on reliability, Antenna checks, ESD cell placement and other layout only features.
- 2005-2006 Integrated graphics (VPG) : SandyBridge (28nm) – first Intel CPU with integrated graphics
- layout design lead, tapeout of Integrated Graphics, owned display block tapeout
  - Convergence of physical design and reliability flows between CPU team (custom approaches) and graphics (ASIC approach) – std cell library, runset, database, fill methodologies, layout database, reliability (EM)
- 1997-2005 (PCI chipsets physical design)
- Broadwater chip set (integrated graphics)
  - Backend lead for Plumas chipset, first server chipset within PCI chipset division.
  - RTL to gates lead for several test chips and validation chips (Intel award)
- 1996-1997 Pre-silicon validation of 440BX chip set – single die North Bridge for Intel CPU
- Defined tests, integrated bus models, wrote full chip tests, owned DRAM testing (no errors in silicon)

**ARM Ltd** (Cambridge, England) 1993 - 1996

- Definition and initial support of AMBA bus standard
- Design of ARM8 integer pipeline (VHDL)
- Support and testing of VHDL wrapper for ARM software model.

**Inmos Ltd** (Bristol, England) 1987 - 1991

- Design of Floating Point Unit for next generation microprocessor (transputer) - performance analysis, algorithm design, definition, hdl design and simulation, custom design and layout of add/subtract unit. Integration into integer pipeline. Formal verification. Synopsys DC used for control logic synthesis.
- Board testing and design completion

**Internship at Ferranti Computer Systems Ltd.**, Bracknell 1983-1986

**Education**

**The Open University (UK)**

Management certificate 1994-1995

**University of Bristol**

B.Eng Computer Systems Engineering (First class honors) 1984-1987

**Chip design tools and skills**

Physical Design.

Antenna (NAC), LVS, DRC, netlisting. Synthesis, Routing, Static timing analysis and timing closure in ASIC environment. Design rules and the underlying process technology. Layer densities, Physical Design for Debug (fiducials, fib cells, spare cells). Fill mechanisms, tech files setup. Tapeouts at 22,14 and 10nm process nodes. Low power design. Formal Verification. Clock tree synthesis.

Power grid design and Reliability

Power grid design and analysis, area vs IR drop, Power gating, EM, on die regulation, bump analysis

Tools and programming

Synopsys ICC, ICV (and Hercules), Synthesis, DC, PrimeTime, Apache Redhawk, verilog, VHDL  
Perl, TCL, C, lisp (emacs macros ..., mainsail)  
Unix, MS word, Excel, Powerpoint. JMP, batch computing

Design

Experience in ASIC design flow from RTL to GDS/OASIS  
Micro-architecture and RTL design of microprocessors  
RTL verification  
Debug and problem solving skills throughout ASIC design flow  
Scripting for design flows and for problem solving.